

REMARKS

In the Office Action of 2/9/2005, claim 1-17 and 28-30 were examined and rejected. In this response, Applicants have canceled claims 29 and 30 and added new claims 36-38. Accordingly, claims 1-17, 28, and 36-38 will be pending in this application.

I. 35 USC 102 Claim Rejections

A. Clams 1-3, 5, 7, 8, 11-14, 17, and 28-30

In the Office Action, the Examiner rejected claims 1-3, 5, 7, 8, 11-14, 17, and 28-30 under 35 USC 102(e) as being anticipated by Hashimoto et al. (US Patent No. 6,344,875, hereinafter Hashimoto).

Claim 1 has been amended and as the rejection may be applied to amended claim 1, respectfully traverse. Amended claim 1 recites a data storage system for a portable data generating appliance comprising:

a temporary data storage circuit coupled, in use, to receive data from the appliance, where the temporary data storage circuit has a storage capacity sufficient to store data comprising at least one picture from the appliance;

a permanent data storage circuit coupled, in use, to receive data from the temporary data storage circuit; and

a control circuit coupled to the temporary data storage circuit and the permanent data storage circuit, wherein the control circuit monitors the amount of time that data is held in the temporary data storage circuit and, after data is held in the temporary data storage circuit for a predetermined time period, causes the data to be transferred to the permanent data storage circuit.

Applicants submit that Hashimoto does not disclose, teach, or even suggest each recited feature of claim 1. For example, Hashimoto does not disclose, teach, or even suggest a temporary data storage circuit that receives data from the appliance, a permanent data storage circuit that receives data from the temporary data storage circuit, and a control circuit that monitors the amount of time that data is held in the temporary data storage circuit and, after data is held in the temporary data storage circuit for a predetermined time period, causes the data to be transferred to the permanent data storage circuit.

Hashimoto discloses (at column 11, lines 45-63 and Figure 16) a process for receiving information by a camera that stores combined image and audio files in a FIFO memory 13 (step 342), separates the combined image and audio information (step 346), and writes the audio and image information into a memory card (step 348). However, Hashimoto does not teach or suggest a control circuit that *monitors the amount of time that data is held in a temporary data storage circuit and, after data is held in the temporary data storage circuit for a predetermined time period,* causes the data to be transferred to the permanent data storage circuit. No where in Hashimoto is it taught or suggested that a control circuit monitors the amount of time that data is held in a temporary data storage circuit and there is simply no use for such a circuit in Hashimoto. Applicants respectfully request that the Examiner specify the precise portion(s) of Hashimoto that disclose such a circuit.

Further, claim 1 requires that after data is held in the temporary data storage circuit for the predetermined time period, the control circuit causes it to be transferred to the permanent data storage circuit. The Examiner states that, in Hashimoto, there are inherent transmission delays from transferring data from the camera to the flash memory 40 through the buffer 41 which are predetermined. However, such an inherent transmission delay occurs during the transfer of data from the camera to the flash memory and does not relate to the prior time period when the data was held in a data storage circuit. The predetermined time period of claim 1, however, relates to a time period that the data is held in the temporary data storage

circuit and does not relate to the transmission delay that may occur after the data is caused to be transferred to the permanent data storage circuit.

In other words, the predetermined time period of claim 1 and the inherent transmission delay cited by the Examiner refer to completely different time periods: the predetermined time period relates to the time period that data is held in the temporary storage whereas the inherent transmission delay cited by the Examiner relates to the delay during transferring of data after it is held in storage. This difference is made most obvious by the fact that “transmission delay” relates to a delay during the transmission or transferring of data, whereas data simply being held in a storage is not being transmitted or transferred and thus does not incur “transmission delay.”

For the above reasons, Applicants submit that amended claim 1 is in allowable form. Claims 2, 3, 5, 7, 8, and 11-14 are dependent upon claim 1, and thus are also allowable for at least the same reasons as claim 1. Independent claims 17 and 28 contain the “monitoring the amount of time” and “predetermined time period” limitations of claim 1 and thus are also in allowable form.

B. Clams 9 and 10

In the Office Action, the Examiner rejected claim 9 under 35 USC 102(e) as being anticipated by Easwar et al. (US Patent Application No. 2001/0036231). The Examiner also rejected claims 9 and 10 under 35 USC 102(e) as being anticipated by Parulski et al. (US Patent Application No. 2001/0013894). Claims 9-10 are dependent upon claim 1, and thus are also allowable for at least the same reasons as claim 1. As discussed above, Hashimoto does not teach or suggest the “monitoring the amount of time” and “predetermined time period” limitations of claim 1. Neither Easwar nor Parulski cure the deficiencies of Hashimoto in teaching or suggesting these limitations.

II. 35 USC 103 Claim Rejections

A. Claim 10

In the Office Action, the Examiner rejected claim 10 under 35 USC 103(a) as being unpatentable over Hashimoto in view of Tringali. Claim 10 is dependent upon claim 1, and thus is allowable for at least the same reasons as claim 1. As discussed above, Hashimoto does not teach or suggest the “monitoring the amount of time” and “predetermined time period” limitations of claim 1. Tringali does not cure the deficiencies of Hashimoto in teaching or suggesting these limitations.

B. Claims 15 and 16

In the Office Action, the Examiner rejected claims 15 and 16 under 35 USC 103(a) as being unpatentable over Hashimoto in view of Levy (US Patent No. 5,438,549). Claims 15 and 16 are dependent upon claim 1, and thus are also allowable for at least the same reasons as claim 1. As discussed above, Hashimoto does not teach or suggest the “monitoring the amount of time” and “predetermined time period” limitations of claim 1. Levy does not cure the deficiencies of Hashimoto in teaching or suggesting these limitations.

C. Claims 4 and 6

In the Office Action, the Examiner rejected claims 4 and 6 under 35 USC 103(a) as unpatentable over Tsukamoto et al. (US Patent Application No. 2002/0048033) in view of Sarkozy et al. (US Patent No. 5,893,919). Claims 4 and 6 are dependent upon claim 1, and thus are also allowable for at least the same reasons as claim 1. As discussed above, Hashimoto does not teach or suggest the “monitoring the amount of time” and “predetermined time period” limitations of claim 1. Neither Tsukamoto nor Sarkozy cure the deficiencies of Hashimoto in teaching or suggesting these limitations.

Further, claim 6 recites the data storage system as claimed in claim 4, wherein:

the permanent data storage circuit comprises a non-volatile
memory module that is *replaceable in the interface card* to allow a

plurality of different memory modules to be used in a single data storage system. (Emphasis added.)

Claim 6 clearly requires that the permanent data storage circuit is replaceable in relation to the interface card. The Examiner states that Tsukamoto discloses a hard disk 701 (Figure 30) in the interface card that is replaceable from within the interface card since the card is manufactured by assembling different components together into a single card and the hard disk is one of the components that can be replaced while being assembled or repaired. Applicants respectfully submit that this definition of a “replaceable” memory module is contrary to how the term is understood in the art. According to the Examiner’s definition, *any* component in any electrical device is a “replaceable” component since the electrical device is manufactured by assembling the different components together. Such a definition renders the term “replaceable” meaningless and is contrary to its usage in the art. As such, claim 6 is allowable for the above reasons as well.

III. New Claims 36-38

New claims 36-38 have been added. These claims are dependent upon claim 28, and thus are also allowable for at least the same reasons as claim 28.

Further, claim 36 recites the method as claimed in claim 28, further comprising:

monitoring whether an erase command is received, wherein said image data is transferred from said temporary data storage circuit to said permanent data storage circuit after the predetermined time period if an erase command is not received during the predetermined time period.

Applicants submit that none of the cited references disclose, teach, or even suggest the additional limitations of claim 36. For example, the cited references do not disclose, teach, or even suggest monitoring whether an erase command is received, wherein image data is transferred from the temporary data storage circuit to the permanent data storage circuit after

the predetermined time period if an erase command is not received during the predetermined time period. Applicants respectfully request that the Examiner specify the precise portion(s) of the cited references that disclose these additional limitations.


CONCLUSION

Based on the foregoing remarks, Applicants believe that the rejections and objections in the Office Action of 2/9/2005 are fully overcome and that the application is in condition for allowance. If the Examiner has any questions regarding the case, the Examiner is invited to contact Applicants' undersigned representative at the number given below.

Respectfully submitted,

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